

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10539334
	Filing Date		2005-06-15
	First Named Inventor	Geetha Arthanari, et al.	
	Art Unit	2825	
	Examiner Name	Suchin Parihar	
	Attorney Docket Number	BUR920020005US1	

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	1	5790841		1998-08-04	Scherer, et al.	
	2	6266803		2001-07-24	Scherer, et al.	
	3	5917729		1999-06-29	Naganuma, et al.	
	4	5610833		1997-03-11	Chang, et al.	
	5	5774371		1998-06-30	Kawakami, et al.	
	6	6223329		2001-04-24	Ling, et al.	
	7	5787268		1998-07-28	Sugiyama, et al.	
	8	6513149		2003-01-28	Donato	
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U.S.PATENT APPLICATION PUBLICATIONS

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	1	20010028265		2001-10-11	Nitta	
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	2	JP2001125037	JP		2001-05-11			<input type="checkbox"/>
	3	JP8044776	JP		1996-02-16			<input type="checkbox"/>
	4	Abstrt 571	JP		1996-05-21			<input checked="" type="checkbox"/>
	5	Abstrt 037	JP		2001-05-11			<input checked="" type="checkbox"/>
	6	Abstrt 776	JP		1996-02-16			<input type="checkbox"/>

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	2	KEITH M. CARRIG, et al - "A Clock Methodology For High-Performance Microprocessors - Journal of VLSI Signal Processing (1997) - pp. 105-111	<input type="checkbox"/>
	3	ANN MARIE RINCON, et al. - "A Proven Methodology for Designing One-Million-Gate ASICs" - IEEE 1996 Custom Integrated Circuits Conference - pp. 45-52	<input type="checkbox"/>

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